We have based our discussion of hazards on Unit 26 of the classical text by C. H. Roth, Jr., *Fundamentals of Logic Design*, 3rd Edition, West Publishing Co., St. Paul, MN, 1985. Even he goes lightly over the discussion of dynamic hazards. A more detailed discussion of this topic can be found in E. J. McCluskey's earlier textbook, *Introduction to the Theory of Switching Circuits*, McGraw-Hill, New York, 1965.

All manufacturers provide data books for their components. The standard reference for TTL components can be obtained from Texas Instruments, the manufacturer that has most popularized the 74XX series. The most critical volumes of their five-volume set are Volume 2, which describes standard, S, and LS TTL, and Volume 3, which describes ALS and AS components.

Exercises

This is not exercise, it's flagellation!

—Noel Coward

3.1 *(Conversion Between Forms)* Use Boolean algebra to verify the following:

a. The AND-OR expression of Figure 3.4 is equivalent to the NAND/NAND expression of that figure.

b. The AND-OR expression of Figure 3.5 is equivalent to the NOR/NOR expression of that figure.

c. The OR/AND expression of Figure 3.6 is equivalent to the NOR/NOR expression of that figure.

d. The OR/AND expression of Figure 3.7 is equivalent to the NAND/NAND expression of that figure.

3.2 *(AND-OR/NAND-NAND Mappings)* Draw schematics for the following expressions, mapped into NAND-only networks. You may assume that literals and their complements are available:

a. $A\overline{B}\overline{C} + \overline{A}C + \overline{A}B$

b. $(\overline{A} + \overline{B} + \overline{C})\ (\overline{A} + \overline{B})\ (\overline{A} + \overline{C})$

c. $\overline{A}B + A + \overline{C} + \overline{D}$

d. $(\overline{A\overline{B}})\ (\overline{\overline{A}\overline{C}})$

e. $\overline{AB + \overline{A}\overline{C}}$

3.3 *(OR-AND/NOR-NOR Mappings)* Draw schematics for the following expressions, mapped into NOR-only networks. You may assume that literals and their complements are available:

a. $(A + B)\ (\overline{A} + C)$

b. $\overline{(A + B) \bullet (\overline{A} + C)}$

c. $\overline{(A + B)} \bullet \overline{(\overline{A} + C)}$

d. $(A+B) \bullet (\overline{A}+C+D) \bullet (\overline{A}+\overline{C})$

e. $(A+B) \bullet (\overline{B} \bullet C) \bullet (\overline{A}+\overline{C})$

3.4 *(Multilevel Network Mappings)* Draw schematics for the following expressions, using mixed NAND and NOR gates only:

a. $(AB+CD)\,E+F$

b. $(AB+C)\,E+DG$

c. $\{A+[(B+C)\,(D+E)]\}\,\{[(F+G)\,(\overline{B}+\overline{E})]+\overline{A}\}$

d. $(A+B)\,(C+D)+EF$

e. $A\overline{B}\,(\overline{B}+C)\,\overline{D}+\overline{A}$

3.5 *(Canonical Forms)* Given the following function in sum of products form (not necessarily minimized):

$$F(A, B, C, D) = \overline{A}BC + AD + AC$$

Reexpress the function in:

a. Canonical product of sums form. Use $\Pi\, M$ notation.

b. Minimized product of sums form.

c. $\overline{F}$ in minimized product of sums form.

d. $\overline{F}$ in minimized sum of products form.

e. Implement F and $\overline{F}$ using NAND gates only. You may assume that literals and their complements are available.

f. Implement F and $\overline{F}$ using NOR gates only. You may assume that literals and their complements are available.

g. Implement F and $\overline{F}$ using a single AND-OR-Invert gate. You may assume that literals and their complements are available.

h. Implement F and $\overline{F}$ using a single OR-AND-Invert gate. You may assume that literals and their complements are available.

3.6 *(AND-OR-Invert Logic)* Implement the following functions using AND-OR-Invert gates. Assume no limitations on inputs or the number of stacks. You may assume that literals and their complements are available.

a. $f(A,B,C) = A \oplus B \oplus C$

b. $f(A,B,C) = AB + BC + AC$

c. $f(A,B,C,D) = \Sigma\, m(1,3,5,7,9) + \Sigma\, d(6,12,13)$

d. $f(A,B,C,D) = \Pi\, M(0,1,6,7)$

e. $f(A,B,C,D) = \Sigma\, m(0,2,4,6)$

3.7 *(OR-AND-Invert Logic)* Implement the same functions as in Exercise 3.4, but this time use OR-AND-Invert gates. Assume no limitations on inputs or the number of stacks. You may assume that literals and their complements are available.

3.8 *(Multilevel Logic)* Factor the following sum of products expressions:

a. $ABCD + ABDE$

b. $ACD + BC + ABE + BD$

c. $AC + ADE + BC + BDE$

d. $AD + AE + BD + BE + CD + CE + AF$

e. $ACE + ACF + ADE + ADF + BCE + BCF + BDE + BDF$

3.9 *(Multilevel Logic)* Write down the function represented by the circuit network in Figure Ex3.9 in a multilevel factored form using AND, OR, and NOT operations only—that is, no NAND or NOR operations:

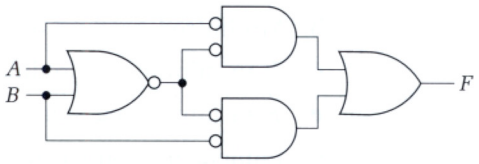


Figure Ex3.9

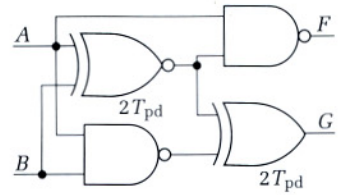
Derive the simplest Boolean expression (minimum number of literals and fewest gates) for the function represented by this schematic. You may use any kind of logic gates described in Chapter 2.

3.10 *(Multilevel Logic)* Using Boolean algebra, K-maps, or truth tables, verify that the multilevel forms for the full adder *Sum* and *CO* (carry-out) obtained in Section 3.1 are logically equivalent to the two-level forms found in Chapter 2.

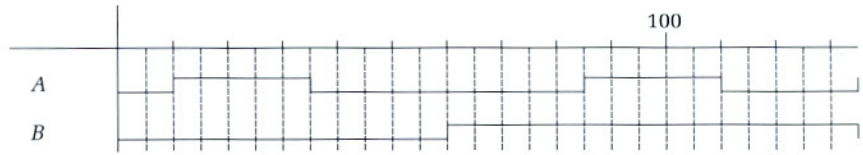
3.11 *(Multilevel Logic)* Using Boolean algebra, K-maps, or truth tables, verify that the multilevel forms for the 2-bit binary adder outputs, X, Y, and Z, of Section 3.1 are logically equivalent to the two-level forms found in Chapter 2.

3.12 *(Multilevel Logic)* Using Boolean algebra, K-maps, or truth tables, verify that the multilevel forms for the BCD increment by 1 outputs, W, X, Y, and Z, of Section 3.1 are logically equivalent to the two-level forms found in Chapter 2.

3.13 *(Time Response)* Consider the circuit in Figure Ex3.13(a). Write down its functions in minimized form. Given that XOR/



(a)

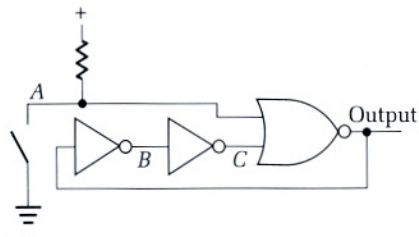


(b)

Figure Ex3.13

XNOR gates have twice the delay of the NAND gates, what is the circuit's output response to the input waveforms in Figure Ex3.13(b)? (Each 5-time-unit division represents one NAND gate delay.)

3.14 *(Time Response)* Consider the circuit with a single input in Figure Ex3.14(a). At time t_0 the switch is moved to the closed (connected) position, and at time t_1 the switch is returned to its original open (disconnected) position. Fill in a timing diagram showing the behavior of the internal signals B and C, and the output signal, in response to this input waveform. Assume all gates have an identical propagation delay T_{pd}, which corresponds to a single division on the chart in Figure Ex3.14(b).



(a)

(b)

Figure Ex3.14

3.15 *(Time Response)* Construct a timing diagram for the behavior of the circuit schematic in Figure Ex3.15.

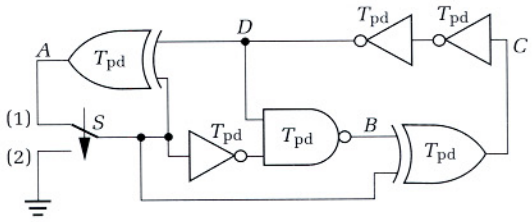


Figure Ex3.15

a. Start by finding a nonoscillating starting condition for the circuit with switch S in position 1 (up) as shown. Fill in the timing waveform with an initial steady-state condition for the circuit nodes labeled *A*, *B*, *C*, and *D*. *Warning:* It is very easy to choose an initial configuration that oscillates. A unique nonoscillating configuration does exist. Start your reasoning with the tightest loop, or make an educated guess and verify that the assumed state is indeed nonoscillating.

b. At time *T*, the switch is moved from position 1 to position 2 (down). Fill in the rest of the timing diagram with the logic values of the signals at points *A*, *B*, *C*, and *D* in the given circuit.

3.16 *(Hazard-Free Design)* Given the following specification of Boolean functions, implement them in a hazard-free manner:

a. $F(A, B, C) = B\overline{C} + \overline{A}C$

b. $F(A, B, C, D) = \Sigma\, m(0, 4, 5, 6, 7, 9, 11, 13, 14)$

c. $F(A, B, C) = (A + B)(\overline{B} + C)$

d. $F(A, B, C, D) = \Pi\, M(0, 1, 3, 5, 7, 8, 9, 13, 15)$

e. $F(A, B, C, D, E) = \Sigma\, m(0, 1, 3, 4, 7, 11, 12, 15, 16, 17, 20, 28)$

3.17 *(TTL Data Book)* To answer this question, you will need access to a TTL data book, preferably one published by Texas Instruments, Inc. Someone has constructed a giant 32-input AND gate from a cascaded tree of 2-input AND gates of type 74S08. This circuit is to drive an output net with 50 picofarads (pF) of capacitance. Assume that the typical capacitance of internal circuit nodes is more like 15 pF. See Figure Ex3.17.

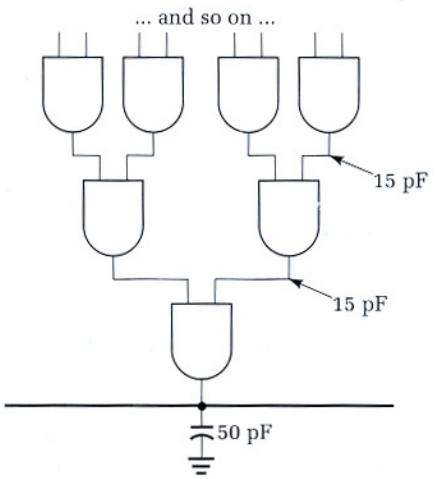


Figure Ex3.17

a. What is the typical average delay through this circuit?

b. What is the typical average DC power consumption of this circuit?

3.18 *(TTL Data Book)* To answer this question, you will need access to a TTL data book. Compute the typical propagation delay and power consumption of the following TTL components:

a. 7400 and 74S00

b. 7402, 74S02, and 74LS02

c. 7404, 74S04, and 74LS04

3.19 *(TTL Data Book)* To answer this question, you will need access to a TTL data book. Compute the following fan-outs:

a. An S TTL NAND gate driving other S TTL NAND gates

b. An LS TTL NAND gate driving S TTL NAND gates

c. A standard TTL NAND gate driving LS TTL NAND gates

d. A standard TTL NAND gate driving S TTL NAND gates

3.20 *(TTL Gates)* It is never a good idea to allow inputs to a TTL gate to "float," that is, to be left unconnected. Give four ways to wire up the unused input of a TTL NAND gate to ensure proper operation of the gate.